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THE ESTABLISHMENT OF A PRODUCTION-READY MANUFACTURING PROCESS UTILIZING THIN SILICON SUBSTRATES FOR SOLAR CELLS

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MOTOROLA REPORT NO. 2364/2
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1 APRIL 1979 - 31 JUNE 1979

JPL CONTRACT NO. 955328

PREPARED BY

R. A. PRYOR

MOTOROLA INC. SEMICONDUCTOR GROUP

5005 EAST McDOWELL ROAD

PHOENIX, ARIZONA 85008

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1.0 SUMMARY

A comparison has been accomplished between several wafer thicknesses and surface conditions. A simple diffused junction structure was used. This structure consists of a phosphine diffused front junction on a p-type substrate with no back surface enhancement. Junction edges were prepared by a mesa etch technique. LPCVD silicon nitride was used for an AR coating and plating mask. The cell back was fully covered with metal. A plated palladium-silver metallization was used for all the test devices in order to eliminate possible dip-soldering difficulties with the thinnest substrates. All test lots but one used substrates which were texture-etched at the start of the process.

The substrate types used are classified as follows: a) polished, 14 mil, 2 Ω-cm; b) as-sawed, 17 mil, 1 Ω-cm; c) as-sawed, 8 mil, 1 Ω-cm; d) chem-etched, 7 mil, 1 Ω-cm; 3) chem-etched, 4 mil, 1 Ω-cm.

Statistical data have been accumulated at each step before, during and after processing. Substrate thickness, substrate resistivity, textured surface peak height, and phosphorus diffusion sheet resistance were measured. Tests were made for open circuit voltage and photo-generation current before AR coat deposition, after AR coat patterning, and after metallization. Current-voltage curves were taken for representative samples.

In general, the electrical performance was found to depend on substrate thickness in exactly the manner predicted by theory. For the simple, non-BSF structure, power conversion efficiency decreases as the substrate is made thinner.

2.0 TECHNICAL PROGRESS

2.1 INITIAL EXPERIMENTAL LOTS

Three inch diameter Czochralski wafers sawed to thicknesses of 17 mils, 8 mils, and 5 mils have been prepared by the Motorola Semiconductor Group Materials Operation. A multiple-wire sawing technology was employed. Some of the 8 mil wafers and all of the 5 mil wafers have been further prepared by chemically etching 0.5 mil of silicon from each side to guarantee removal of sawing damage. Statistical measurements on this material were reported in Technical Quarterly Report No. 1. A number of these wafers, along with some control wafers produced by Wacker, were used to establish the first six test lots for thin cell fabrication. The cells produced in these lots will provide a baseline for judging cell performance and processing improvements directed toward incorporating thin substrates into production processing.

Each test lot was started with 24 wafers per lot. This number allows a space position for a test wafer in the standard carriers and diffusion boats which hold 25 wafers. Each of the six test lots is described in the following paragraphs. Each starting wafer in each of the six lots has been measured to determine wafer resistivity and thickness at the wafer center. All wafers are Czochralski material.

Lot A1 is a control. It contains wafers produced by Wacker which are chemically etched on the back and polished on the front. The average wafer resistivity is 2.34 Ω-cm (σ = 0.10 Ω-cm) and the average center thickness is 14.28 mils (σ = 0.21 mils).

Lot A2 contains wafers from crystals grown at Motorola; they are in the as-cut condition and are edge rounded. The average wafer resistivity is 1.01 Ω-cm (σ = 0.11 Ω-cm) and the average thickness at the center is 17.74 mils (σ = 0.19 mils).

Lot A3 is a lot of thin, as-cut wafers grown and cut at Motorola. These wafers are not edge rounded. The average wafer resistivity is 1.30 Ω-cm (σ = 0.02 Ω-cm) and the average center thickness is 8.24 mils (σ = 0.20 mils).

A4 is a lot of thin wafers sliced at Motorola to approximately 5 mils and then chemically thinned to eliminate saw damage. Average wafer resistivity is 1.20 Ω-cm (σ = 0.04 Ω-cm) and the average center thickness is 4.39 mils (σ = 0.05 mils).

A5 is a lot of thin wafers sliced at Motorola to approximately 8 mils, edge rounded, and then chemically etched. The average wafer resistivity is 1.44 Ω-cm (σ = 0.19 Ω-cm) and the average center thickness is 7.22 mils (σ = 0.11 mils).

Lot A6 is identical to lot A5 in starting condition. The average wafer resisitivity is 1.51 Ω-cm (σ = 0.19 Ω-cm) and the average center thickness is 7.09 mils (σ = 0.09 mils).

Detailed tabulations of resistivity and starting thickness measurements for each lot will be presented as part of the data in Section 2.3.

With the exception of surface texturing, all six lots were processed through the same junction formation, antireflection coating, and metallization steps. The wafers in lots A1, A2, A3, A4, and A5 have been textured on both sides using the standard Motorola texture etch process. As a result, lots A1 and A2 have textured peaks with a nominal height of 7 microns, lot A3 has textured peaks nominally 6.5 microns high, and lots A4 and A5 have textured peaks nominally 5 microns high.

Each wafer in each lot was measured after texturing to determine wafer thickness loss. The average "peak-to-peak" thickness loss from before to after texturing ranged from 4.8 microns to 7.6 microns. Thickness measure-

TABLE 1: SUMMARY OF THE COMPOSITION AND SUBSTRATE CHARACTERISTICS FOR TEST LOTS A1 THROUGH A6.

LOT NUMBER	LOT FUNCTION	AVERAGE STARTING THICKNESS (mils)	STARTING WAFER CONDITION	PROCESSED SURFACE CONDITION	LOT RESISTIVITY RANGE (Ω-cm)	WAFER MANUFACTURER
A2	control	17.7	as-sawed*, edge-rounded	textured	0.87-1.12	Motorola
A3	test	8.2	as-sawed*	textured	1.26-1.33	Motorola
A5	test	7.2	chem-etched, edge-rounded	textured	1.18-1.73	Motorola
A4	test	4.4	chem-etched	textured	1.17-1.37	Motorola
A6	test	7.1	chem-etched, edge-rounded	as-started	1.15-1.70	Motorola
A1	control	14.3	polished front, chem-smoothed back	textured	2.12-2.49	Wacker

*as-sawed using multiple wire saw technology

ments were performed with a stage micrometer, so measurements with textured surfaces reflect the distance from textured peaks on one side to the tips of textured peaks on the other side. Thickness data after texture are also tabulated in Section 2.3.

Lot A6 was not textured and has been retained in the smooth, chemically etched surface condition.

Table 1 summarizes the substrate characteristics for each of the six test lots.

2.2 INITIAL PROCESS SEQUENCE

The initial six test lots of thin substrate solar cells were processed with the following process sequence:

1. Start with sawed or sawed and etched wafers as procurred from Materials Operation.
2. Clean wafers in hot piranha solution (a mixture of sulfuric acid and hydrogen peroxide), rinse, etch in dilute HF solution, rinse.
3. Texture etch both sides of wafers and rinse (excluding lot A6).
4. Dry wafers using Freon vapor "degreaser" technique.
5. Plasma oxidation/clean ("ashing").
6. PH_3 diffusion, both sides, at 900°C for approximately 18 minutes.
7. Strip phosphorus glass in HF and rinse.
8. Dry wafers using Freon vapor "degreaser" technique.
9. Mesa etch front perimeter and etch back to remove phosphorus layer. This is done with a standard photoresist procedure to protect the desired junction from the silicon etch (nitric-hydrofluoric-acetic acid mixture).
10. Plasma oxidation/clean.

11. LPCVD Si_3N_4 deposition.

12. Etch front metal pattern, stripping back surface Si_3N_4 layer.

13. Metallize.

In step 13, to eliminate initial concern for stress in using a solder coating process for the metal contact, a plated palladium-silver metallization system was used for lots A1 through A6.

In step 4 of the process sequence listed above, wafers are dried in the following manner. After rinsing, a carrier of wet wafers is placed in a container of isopropal alcohol which displaces and mixes with the water on the wafer surface. The carrier is then placed in the hot vapor section of a Freon vapor degreaser. The hot Freon vapor condenses on the colder wafer surfaces and drips off the wafers to the liquid sump below, carrying any particulate residue away. As the carrier of wafers is withdrawn from the vapor, the Freon remaining on the wafer surface evaporates, leaving the wafers dry. This drying process was originally chosen because it provides a very gentle method for drying the thin substrates. However, it has since been determined with other experiments that conventional centrifugal spin-drying can be used, even for the 4 mil substrates, without substantial risk of breakage.

In step 11 of the process sequence, LPCVD silicon nitride deposition refers to a low pressure chemical vapor deposition process whereby a uniform Si_3N_4 film is deposited on both sides of the solar cell substrate at pressures below atmospheric pressure. The nitride film thickness is such as to serve both as a metal plating mask and as a front surface antireflection coating. This process provides superior uniformity and reliability with excellent throughput.

Plasma oxidations were introduced in steps 5 and 10 as the first effort to eliminate some of the wafer handling involved in using wet chemical cleans

and rinses prior to high temperature furnace operations. Using the dry plasma process requires less handling and is more gentle with respect to breakage of very thin silicon substrates.

Pertinent data were taken for each wafer in lots A1 through A6 after each major step in the process sequence. Junction sheet resistances were measured for the phosphorus diffused layer after completing step 8. Photogeneration current was measured after step 9 by using a diode curve-tracer to observe the solar cell reverse-biased characteristic I-V curve under simulated AM1 illumination. The illumination was provided by a quartz-halogen lamp source and calibrated with a reference cell fabricated by JPL.

These in-process data are given in the detailed tabulations to be found in Section 2.3. Wafer loss through in-process breakage was also recorded and this information was used to calculate cumulative yields after major process steps.

2.3 EXPERIMENTAL RESULTS

2.3.1 BASELINE CELL STRUCTURE

As a result of the process sequence described in Section 2.2, the baseline solar cell structure is a very basic n-on-p configuration. This is similar to what might be used if one were choosing a structure for the least expensive fabrication costs with today's technology.

Of the six lots discussed in this report, five consisted of wafers which were textured, both front and back, at the onset of processing. One lot was not textured, but was chemically etched to smooth the as-sawed surface.

The n-type front surface junction layer was formed with a phosphorus diffusion (from a PH_3 source) followed by a mesa etch process. The mesa etch process strips the unwanted diffused layer from the back of the substrate and from a ring around the edge of the cell front. Those areas which have been

etched to remove phosphorus are smoothed considerably compared to the original sharp-edged textured surface but still retain tetrahedral shapes. The resulting p-n junction area is 43.3 cm^2. The average junction depth for lots A1 through A6 is near 0.6 μm. No back surface enhancement diffusion (p+ layer) or back surface field (BSF) was employed for these lots.

The completed solar cells have an antireflection coating of silicon nitride (Si_3N_4). This coating is applied to both sides of the cell substrate before metallization. A low pressure chemical vapor deposition (LPCVD) system characteristically coats both sides of the wafers being processed. Average Si_3N_4 coating thickness for the six test lots is 744Å.

A metal plating mask is formed with the Si_3N_4 by stripping the back surface of the wafer and patterning the front with a metal grid pattern. Thus, the completed cells have metal totally covering the back surface. The front surface grid shadows approximately 8% of the p-n junction area.

As previously stated, the metallization used for lots A1 through A6 consists of a palladium-palladium silicide contact layer and a silver conducting layer. This system was chosen because it was available and because the 4 mil substrates could be safely plated without concern for breakage likely to be encountered if a solder-dip process were chosen. Unfortunately, the front surface grid pattern used is optimized for a soldered metallization. The amount of shadowing could be reduced if the pattern were optimized for silver instead. With the pattern used and the silver conductor, the total series resistance of the cell is typically about 5 milliohms. This corresponds to a voltage loss of about 6 mV at an output current of 1200 mA.

2.3.2 LOT DATA SUMMARY

Important parameters and experimental results for the baseline cell test lots are summarized in Table 2. Where items are labeled average they are the mean value of measurements taken on all the cells in a given lot.

The as-processed wafer thickness is the measured "peak-to-peak" wafer thickness after texturing except for lot A6, which is not textured. This measurement was discussed in Section 2.1. The textured surface peak size is an estimate (by optical microscopy) of the largest typical distance from the base of the silicon surface tetrahedra to the peak.

The open circuit voltage (V_{OC}) and short circuit current (I_{SC}) values represent measurements on the completed solar cells. V_{OC} measurements were made with a digital voltmeter and I_{SC} values were read from a curve-tracer display. All such measurements were made under tungsten-quartz-halogen lamp (type ENH) illumination set to an insolation of 100 mW/cm^2 by a JPL-calibrated reference cell (No. MO-04).

The maximum power (P_{max}) data represent values taken from current-voltage characteristic curve plots which will be given in Section 2.3.3.

Processing yield is simply the number of completed solar cells left intact per lot divided by 24, the number of wafers started per lot. The yield loss is strictly a result of wafer breakage. Two notes of caution must be given for interpreting the yield numbers. First, these lots represent the first attempt to process substrates of such thinness and must be expected to suffer somewhat from inexperience. As more experience is obtained and as processing is altered to accomodate the special nature of thin substrates, yield will be improved. Second, the wafers in these lots were subjected to an extra measure of prodding and probing by trying to accumulate substantial

TABLE 2: SUMMARY OF IMPORTANT LOT PARAMETERS AND EXPERIMENTAL RESULTS.

LOT NUMBER	AVERAGE WAFER THICKNESS AS-PROCESSED (mils)	TEXTURED SURFACE PEAK SIZE (μm)	AVERAGE WAFER RESISTIVITY (Ω-cm)	AVERAGE V_{OC} (mV)	AVERAGE I_{SC} (mA)	REPRESENTATIVE P_{max} (mW)	1st ATTEMPT PROCESSING YIELD (%)
A2	17.44	7	1.01	602	1306	629	100
A3	7.95	6.5	1.30	586	1251	580	91.7
A5	7.03	5	1.44	592	1286	595	95.8
A4	4.18	5	1.20	578	1185	550	66.7
A6	7.09	not textured	1.51	586	1234	569	91.7
A1	14.09	7	2.34	576	1284	586	83.3

amounts of in-process data. This increases the amount of handling and increases the chance for initiating fractures. Such data accumulation would not ordinarily be done for routine cell production.

2.3.3 DETAILED DATA PRESENTATION

The data summarized in Table 2 are given in detail at the end of this seciton in Tables 3 through 8 and Figures 1 through 6 for lots A1 through A6, respectively. In addition, Tables 3 through 8 list measurements of starting substrate thickness, phosphorus diffused layer sheet resistance, and solar cell photo-generation current obtained before antireflection coating and metallization are applied. For each set of data tabulated, the statistical mean, standard deviation, and percent standard deviation are given. Percent standard deviation is the standard deviation divided by the mean and multiplied by 100.

Each of the current-voltage curves given in Figures 1 through 6 represents a sample from lots A1 through A6, respectively. Data taken and computed from the curves include V_{OC} , I_{SC}, maximum power voltage (V_{mp}), maximum power current (I_{mp}), P_{max}, power conversion efficiency (η), and curve fill factor (CFF). Efficiency numbers are based on the total area of a three inch diameter silicon wafer with flats (45.35 cm^2), for which the junction mesa pattern and the metallization grid pattern are designed. If only the p-n junction area (including metal shadowing) were considered, or if the junction were formed to the edge of the wafer, the efficiency values given would be increased by an additional 0.6% (i.e., η = 13.9% would become η = 14.5%).

TABLE 3: Wafer data for test lot no. A1

WAFER NUMBER	STARTING THICKNESS (mils)	WAFER RESISTIVITY (Ω-cm)	THICKNESS AFTER TEXTURE (mils)	JUNCTION SHEET RESISTANCE (Ω/□)	BARE SURFACE GENERATION CURRENT (mA)	COMPLETED CELL SHORT CIRCUIT CURRENT I_{SC} (mA)	COMPLETED CELL OPEN CIRCUIT VOLTAGE V_{OC} (mV)
1	13.91	2.47	13.93	33.2	1230	1300	579
2	14.15	2.34	13.94	33.9	1240	1300	575
3	14.06	2.27	13.82	31.9	1230	1300	577
4	14.40	2.41	14.25	34.0	1240	1280	575
5	13.97	2.39	13.81	---	---	---	---
6	14.33	2.42	14.12	31.0	1230	1280	576
7	14.43	2.49	14.27	34.8	1230	1280	575
8	14.22	2.30	14.10	31.6	1230	1280	577
9	14.48	2.29	14.31	32.3	1220	1280	577
10	14.50	2.44	14.37	35.6	1220	1280	574
11	14.42	2.30	14.21	31.6	1220	1280	576
12	14.07	2.37	13.90	29.0	1230	1280	575
13	14.47	2.33	14.29	33.6	1210	1280	574
14	14.23	2.44	14.10	31.0	1220	1270	574
15	14.55	2.48	14.40	31.6	1230	1270	573
16	14.43	2.17	14.26	31.1	1220	1280	577
17	14.16	2.29	14.00	33.2	1220	1280	573
18	14.68	2.36	14.51	30.2	1230	1300	577
19	14.20	2.12	14.05	31.5	1230	---	---
20	13.93	2.29	13.74	31.7	1240	1280	575
21	14.41	2.36	13.85	29.5	1240	1290	577
22	14.18	2.37	13.90	30.1	1250	---	---
23	14.38	2.38	14.21	31.3	1250	---	---
24	14.04	2.19	13.84	30.2	1270	1290	574
MEAN	14.28	2.34	14.09	32.0	1232	1284	576
STD. DEV.	0.21	0.10	0.22	1.7	13	9	2
% STD. DEV.	1.5%	4.1%	1.5%	5.3%	1.1%	0.7%	0.3%
CUMULATIVE YIELD	N.A.	N.A	100%	95.8%	95.8%	---	83.3%

TABLE 4: Wafer data for test lot no. A2

WAFER NUMBER	STARTING THICKNESS (mils)	WAFER RESISTIVITY (Ω-cm)	THICKNESS AFTER TEXTURE (mils)	JUNCTION SHEET RESISTANCE (Ω/□)	BARE SURFACE GENERATION CURRENT (mA)	COMPLETED CELL SHORT CIRCUIT CURRENT I_{SC} (mA)	COMPLETED CELL OPEN CIRCUIT VOLTAGE V_{OC} (mV)
1	17.82	0.89	17.28	32.4	1220	1290	607
2	17.68	0.88	17.22	32.0	1210	1300	605
3	17.82	0.87	17.41	33.5	1200	1310	605
4	17.67	0.88	17.35	33.7	1200	1310	605
5	17.58	0.89	17.32	32.9	1200	1300	603
6	17.63	0.87	17.39	33.9	1190	1300	603
7	17.51	0.88	17.27	31.9	1190	1300	603
8	17.50	0.88	17.28	34.6	1190	1310	605
9	17.68	0.89	17.28	32.0	1180	1300	602
10	17.89	0.88	17.43	34.0	1200	1300	604
11	17.77	1.09	17.55	31.1	1200	1300	599
12	17.96	1.12	17.70	32.0	1200	1310	600
13	18.10	1.11	17.68	34.0	1220	1320	601
14	17.79	1.12	17.48	31.5	1200	1320	600
15	17.58	1.09	17.35	31.3	1200	1310	600
16	17.94	1.10	17.71	32.7	1200	1310	599
17	18.07	1.10	17.79	29.8	1190	1300	599
18	17.65	1.08	17.43	30.3	1200	1300	598
19	17.59	1.10	17.38	31.0	1210	1310	600
20	17.62	1.04	17.35	28.4	1210	1310	600
21	17.59	1.09	17.37	31.7	1200	1310	600
22	17.60	1.08	17.35	28.9	1200	1310	601
23	17.70	1.12	17.38	28.6	1220	1310	600
24	18.13	1.10	17.75	28.0	1200	1310	599
MEAN	17.74	1.01	17.44	31.8	1201	1306	602
STD. DEV.	0.19	0.11	0.17	1.8	10	7	3
% STD. DEV.	1.1%	10.9%	1.0%	5.6%	0.8%	0.5%	0.4%
CUMULATIVE YIELD	N.A.	N.A.	100%	100%	100%	---	100%

TABLE 5: Wafer data for test lot no. A3

WAFER NUMBER	STARTING THICKNESS (mils)	WAFER RESISTIVITY (Ω-cm)	THICKNESS AFTER TEXTURE (mils)	JUNCTION SHEET RESISTANCE (Ω/□)	BARE SURFACE GENERATION CURRENT (mA)	COMPLETED CELL SHORT CIRCUIT CURRENT I_{SC} (mA)	COMPLETED CELL OPEN CIRCUIT VOLTAGE V_{OC} (mV)
1	8.83	1.28	8.45	54.6	1240	---	---
2	8.06	1.27	7.81	46.5	1240	1270	588
3	8.31	1.26	8.05	40.3	1230	1250	586
4	8.60	1.28	8.28	---	---	---	---
5	8.31	1.30	8.03	56.4	1240	1250	586
6	8.08	1.30	7.82	63.4	1240	1220	579
7	8.30	1.26	8.05	54.3	1240	1260	586
8	8.50	1.28	8.20	64.6	1220	1280	588
9	8.22	1.30	7.92	55.8	1230	1260	586
10	8.03	1.32	7.76	46.5	1230	1250	585
11	8.09	1.32	7.82	52.8	1230	1260	586
12	8.08	1.31	7.80	52.0	1230	1250	586
13	8.14	1.32	7.89	50.5	1220	1250	585
14	8.20	1.30	7.95	48.7	1240	1250	586
15	8.28	1.27	8.00	47.2	1240	1250	586
16	8.31	1.31	8.03	44.6	1240	1240	586
17	8.42	1.31	7.99	54.9	1240	1240	585
18	8.12	1.33	7.85	45.8	1230	1260	587
19	8.06	1.32	7.80	44.0	1240	1240	577
20	8.08	1.31	7.81	45.1	1230	1250	585
21	8.25	1.31	7.98	40.3	1230	1250	586
22	8.12	1.31	7.90	40.0	1230	1250	586
23	8.06	1.33	7.75	37.6	1240	1250	586
24	8.25	1.29	7.97	37.1	1210	1240	585
MEAN	8.24	1.30	7.95	49.4	1233	1251	586
STD. DEV.	0.20	0.02	0.17	7.3	8	12	2
% STD. DEV.	2.4%	1.6%	2.1%	14.8%	0.7%	1.0%	0.3%
CUMULATIVE YIELD	N.A.	N.A.	100%	95.8%	95.8%	---	91.7%

TABLE 6: Wafer data for test lot no. A4

WAFER NUMBER	STARTING THICKNESS (mils)	WAFER RESISTIVITY (Ω-cm)	THICKNESS AFTER TEXTURE (mils)	JUNCTION SHEET RESISTANCE (Ω/□)	BARE SURFACE GENERATION CURRENT (mA)	COMPLETED CELL SHORT CIRCUIT CURRENT I_{SC} (mA)	COMPLETED CELL OPEN CIRCUIT VOLTAGE V_{OC} (mV)
1	4.35	1.37	4.13	39.1	1220	1170	575
2	4.38	1.19	4.16	43.6	1280	---	---
3	4.36	1.24	4.12	41.4	1280	---	---
4	4.39	1.20	4.17	39.4	1240	1180	579
5	4.40	1.20	4.20	39.2	1240	1180	578
6	4.41	1.20	4.20	36.5	1250	1180	578
7	4.39	1.17	4.17	40.8	1300	1190	578
8	4.40	1.20	4.16	38.2	1270	1190	577
9	4.43	1.18	4.22	39.2	1260	1200	578
10	4.37	1.20	4.18	42.3	1220	1190	577
11	4.47	1.20	4.25	38.0	1230	1180	578
12	4.50	1.18	4.29	36.8	1260	1180	579
13	4.50	1.17	4.23	37.7	1230	---	---
14	4.36	1.17	4.15	36.5	1220	1180	578
15	4.33	1.18	4.19	37.2	1220	1180	576
16	4.39	1.21	4.19	35.7	1220	1190	578
17	4.32	1.20	4.12	36.1	1240	1190	577
18	4.40	1.23	4.19	35.8	1210	1190	576
19	4.34	1.24	4.14	35.0	---	---	---
20	4.43	1.18	4.20	33.0	1230	1190	578
21	4.43	1.20	4.23	---	---	---	---
22	4.28	1.18	4.09	29.6	1240	---	---
23	4.42	1.23	---	---	---	---	---
24	4.39	1.19	---	---	---	---	---
MEAN	4.39	1.20	4.18	38.1	1243	1185	578
STD. DEV.	0.05	0.04	0.05	2.6	25	7	1
% STD. DEV.	1.2%	3.4%	1.1%	6.7%	2.0%	0.6%	0.2%
CUMULATIVE YIELD	N.A.	N.A.	91.7%	87.5%	83.3%	---	66.7%

TABLE 7: Wafer data for test lot no. A5

WAFER NUMBER	STARTING THICKNESS (mils)	WAFER RESISTIVITY (Ω-cm)	THICKNESS AFTER TEXTURE (mils)	JUNCTION SHEET RESISTANCE (Ω/□)	BARE SURFACE GENERATION CURRENT (mA)	COMPLETED CELL SHORT CIRCUIT CURRENT I_{SC} (mA)	COMPLETED CELL OPEN CIRCUIT VOLTAGE V_{OC} (mV)
1	7.15	1.36	7.00	34.8	1340	1270	596
2	7.29	1.35	7.05	35.7	1280	1270	594
3	7.10	1.41	6.93	37.1	1280	1270	593
4	7.18	1.41	7.02	36.4	1320	1280	593
5	7.10	1.36	6.97	37.2	1300	1290	594
6	7.16	1.39	6.98	38.3	1280	1280	594
7	7.17	1.67	7.00	39.5	1290	1280	588
8	7.14	1.68	6.99	38.4	1300	1290	588
9	7.01	1.18	6.82	39.6	1270	---	---
10	7.18	1.69	6.93	38.2	1280	1280	588
11	7.17	1.24	6.98	41.1	1260	1280	594
12	7.16	1.21	6.98	41.8	1240	1280	595
13	7.12	1.25	6.95	38.8	1250	1280	594
14	7.35	1.42	7.18	41.6	1240	1290	593
15	7.49	1.73	7.16	44.9	1260	1290	588
16	7.39	1.68	7.21	43.0	1250	1290	590
17	7.26	1.64	7.10	43.2	1260	1290	588
18	7.25	1.64	7.09	43.9	1270	1290	588
19	7.22	1.68	7.05	45.3	1260	1300	588
20	7.23	1.37	7.05	46.6	1260	1290	592
21	7.36	1.37	7.09	44.4	1280	1290	592
22	7.22	1.32	7.05	51.9	1270	1300	593
23	7.26	1.20	7.08	52.7	1260	1300	593
24	7.29	1.25	7.00	44.6	1230	1290	593
MEAN	7.22	1.44	7.03	41.5	1272	1286	592
STD. DEV.	0.11	0.19	0.09	4.7	25	9	3
% STD. DEV.	1.5%	12.9%	1.2%	11.4%	2.0%	0.7%	0.5%
CUMULATIVE YIELD	N.A.	N.A.	100%	100%	100%	---	95.8%

TABLE 8: Wafer data for test lot no. A6

WAFER NUMBER	STARTING THICKNESS (mils)	WAFER RESISTIVITY (Ω-cm)	THICKNESS AFTER TEXTURE (mils)	JUNCTION SHEET RESISTANCE (Ω/□)	BARE SURFACE GENERATION CURRENT (mA)	COMPLETED CELL SHORT CIRCUIT CURRENT I_{SC} (mA)	COMPLETED CELL OPEN CIRCUIT VOLTAGE V_{OC} (mV)
1	7.23	1.69	NOT APPLICABLE	36.9	970	1200	582
2	7.30	1.70		36.4	960	1220	585
3	7.32	1.42		36.9	970	1230	587
4	7.08	1.33		37.7	960	1230	589
5	7.11	1.33		37.4	970	1220	589
6	6.95	1.24		37.8	960	1230	591
7	7.06	1.30		39.2	960	1230	590
8	6.98	1.23		39.9	950	1230	591
9	7.06	1.37		38.7	980	1240	589
10	7.02	1.62		40.4	960	1240	587
11	7.00	1.15		37.9	950	1240	592
12	7.06	1.67		41.5	960	1240	583
13	7.13	1.69		39.3	960	1250	586
14	7.08	1.61		39.7	960	1240	580
15	7.04	1.61		38.5	980	1250	586
16	7.12	1.62		42.1	970	1240	585
17	7.09	1.61		40.1	970	*	587
18	7.02	1.67		41.2	950	*	582
19	7.11	1.69		35.8	930	---	---
20	7.08	1.70		41.5	970	*	586
21	7.06	1.31		43.8	940	---	---
22	7.07	1.32		44.6	940	*	587
23	7.14	1.61		47.2	950	1250	578
24	7.09	1.65		45.6	960	1240	577
MEAN	7.09	1.51		39.8	960	1234	586
STD. DEV.	0.09	0.19		2.8	12	12	4
% STD. DEV.	1.2%	12.4%		7.0%	1.3%	1.0%	0.7%
CUMULATIVE YIELD	N.A.	N.A.	N.A.	100%	100%	---	91.7%

A1 #8
461510

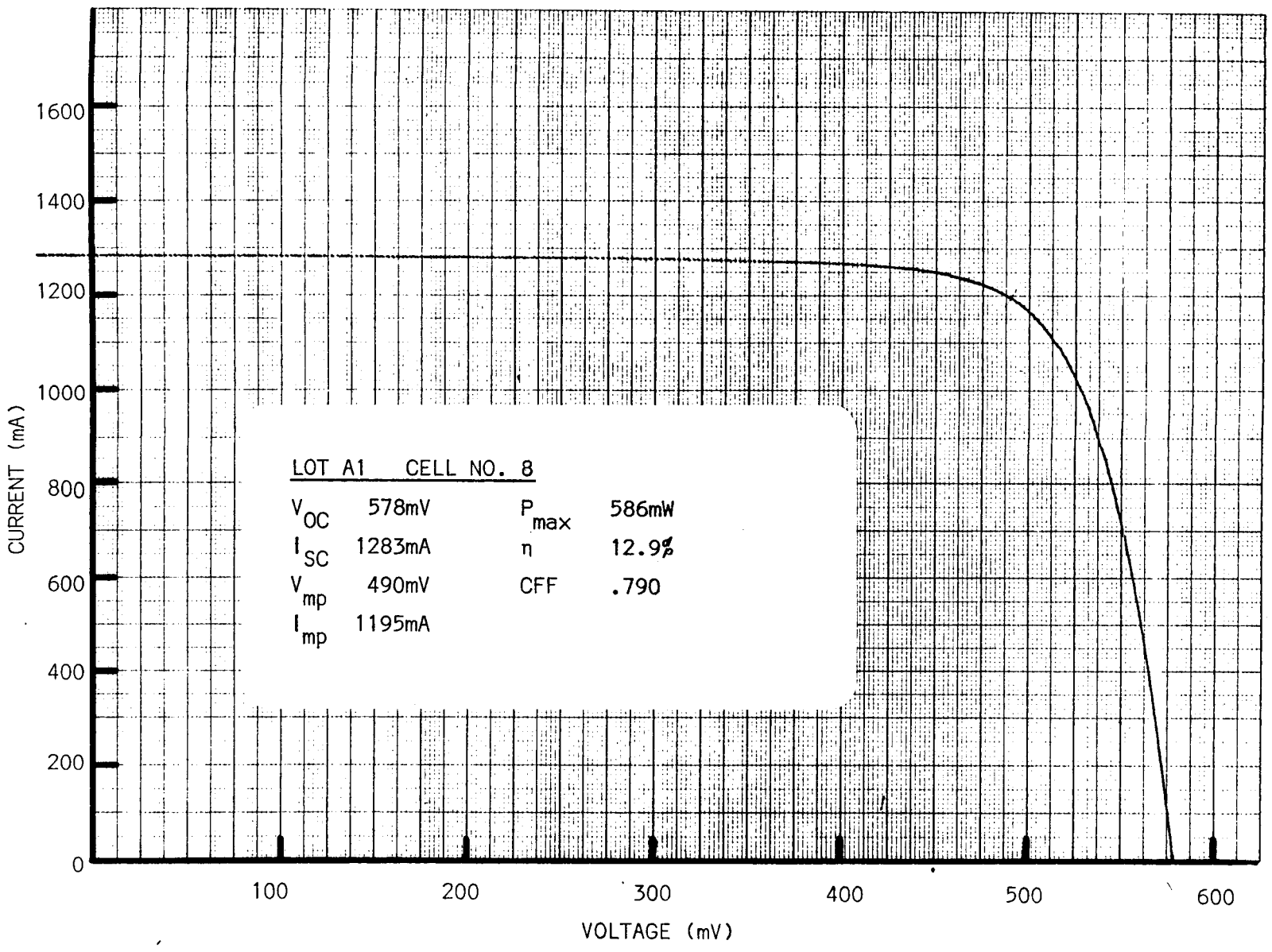

FIGURE 1: Representative AM1 current-voltage response curve for test lot no. A1

A2 #12
461510

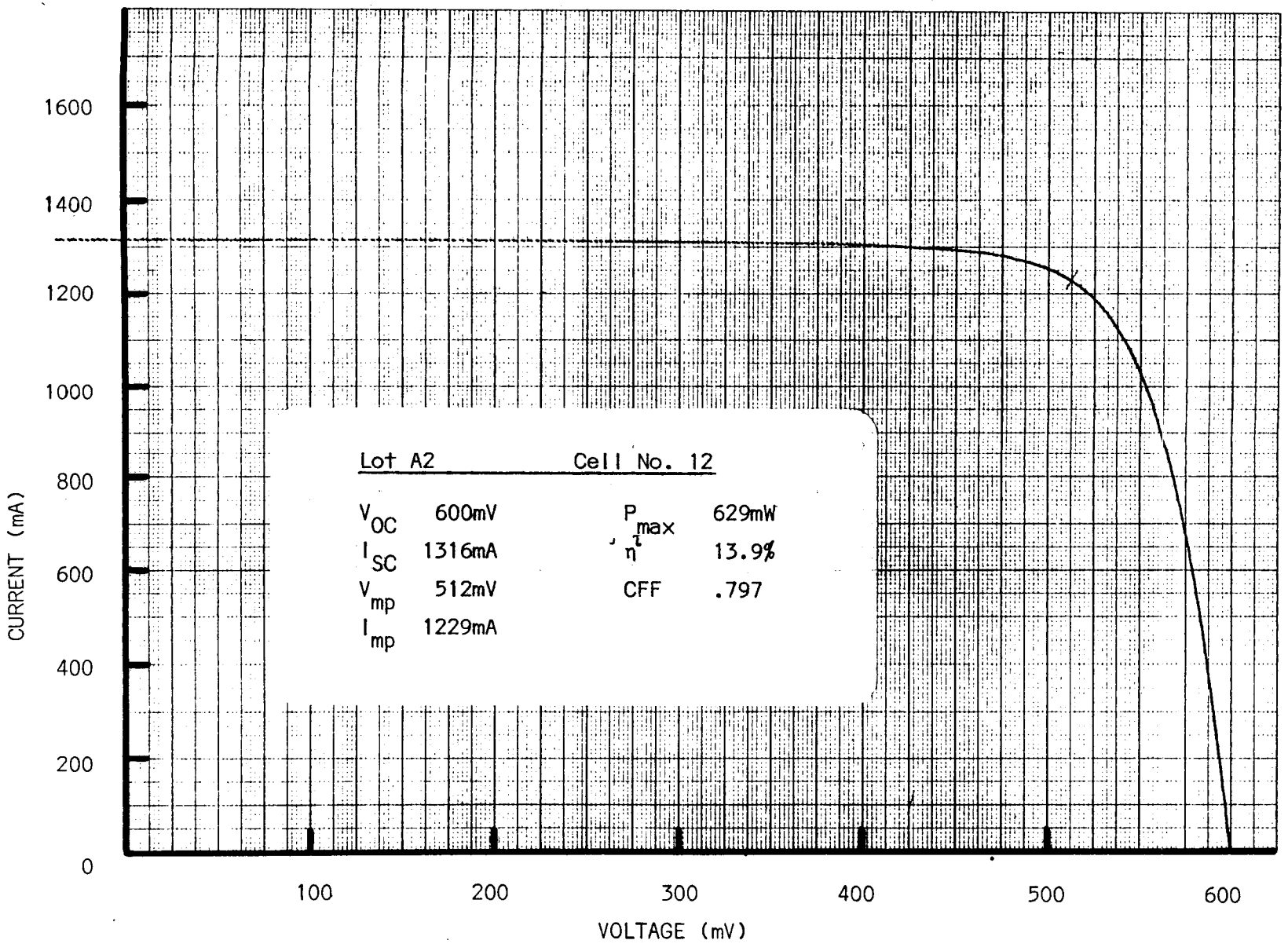

FIGURE 2: Representative AM1 current-voltage response curve for test lot no A2

A3 # 18
461510

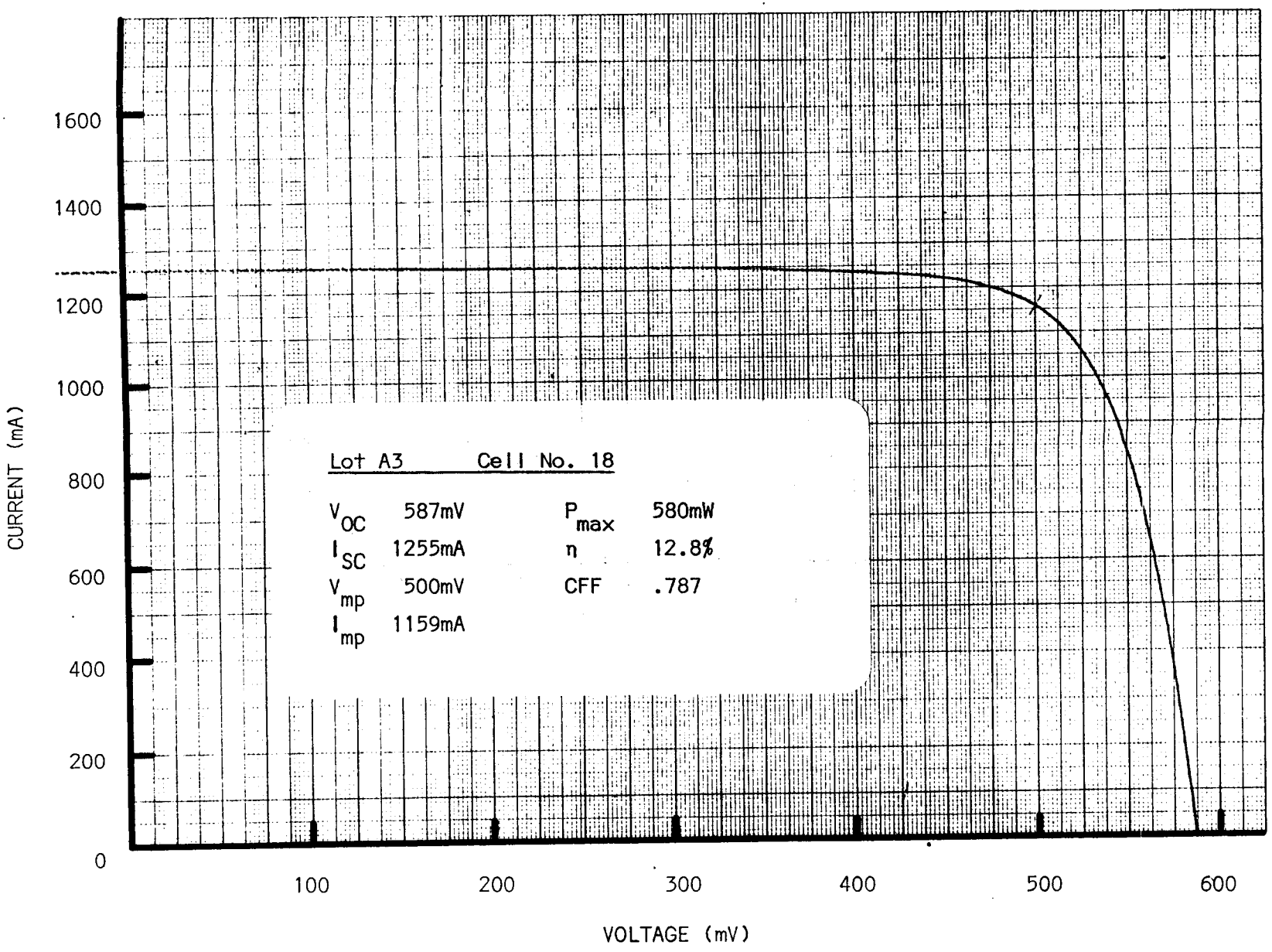

FIGURE 3: Representative AM1 current-voltage response curve for test lot no. A3.

A4 #9
461610

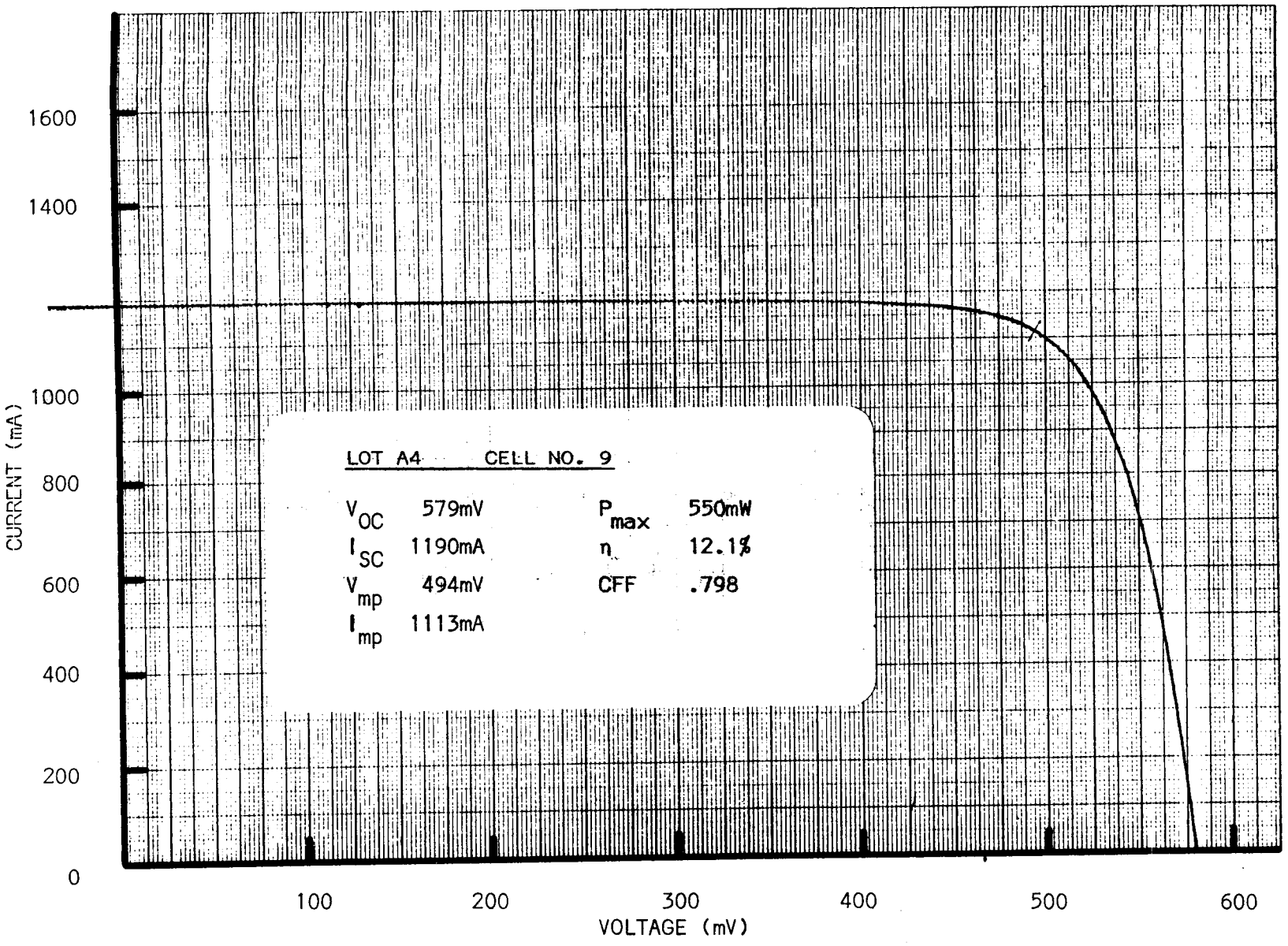

FIGURE 4: Representative AM1 current-voltage response curve for test lot no. A4.

A5 #10
461510

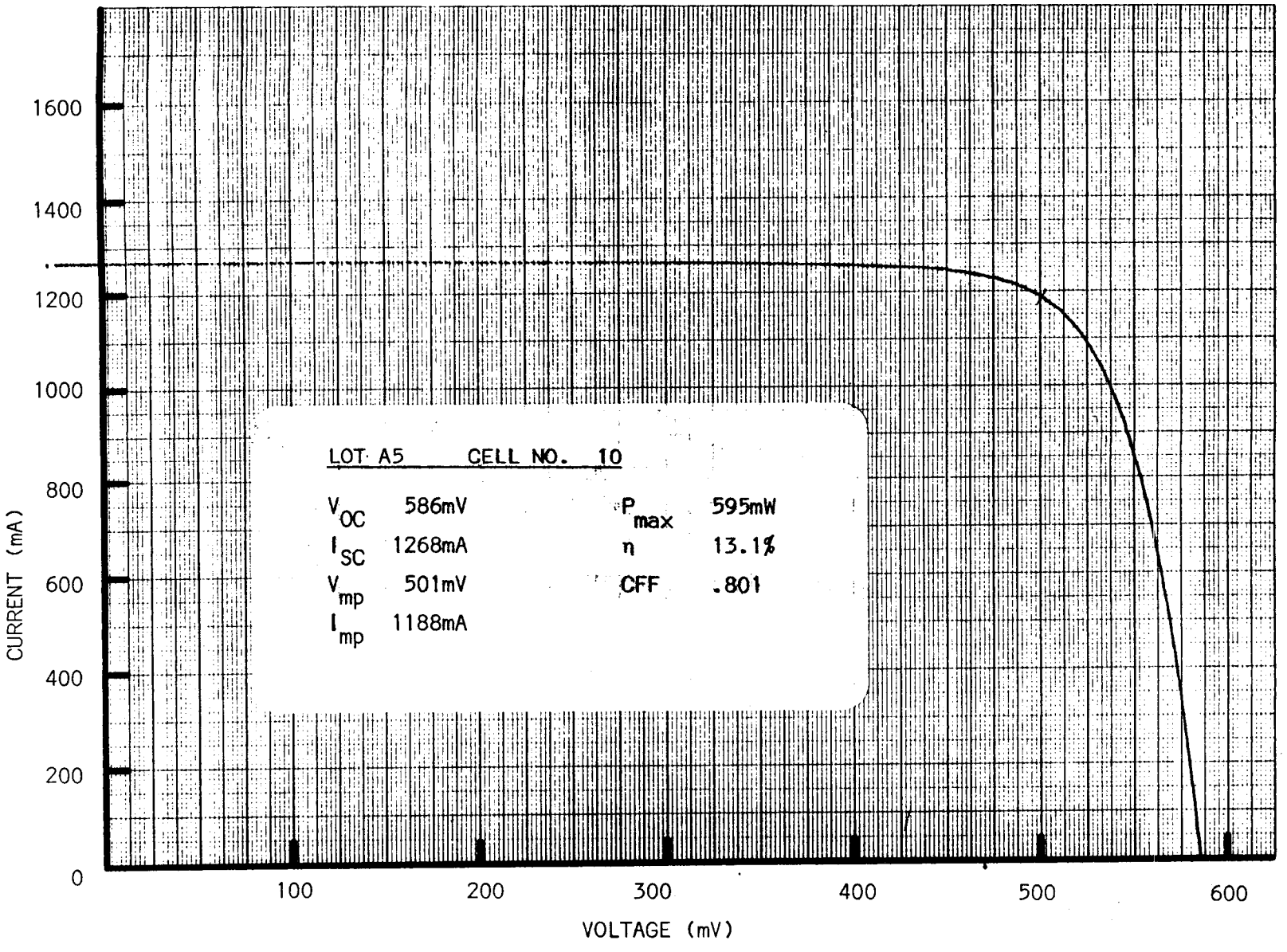

FIGURE 5: Representative AM1 current-voltage response curve for test lot no. A5.

A6 #13
461510

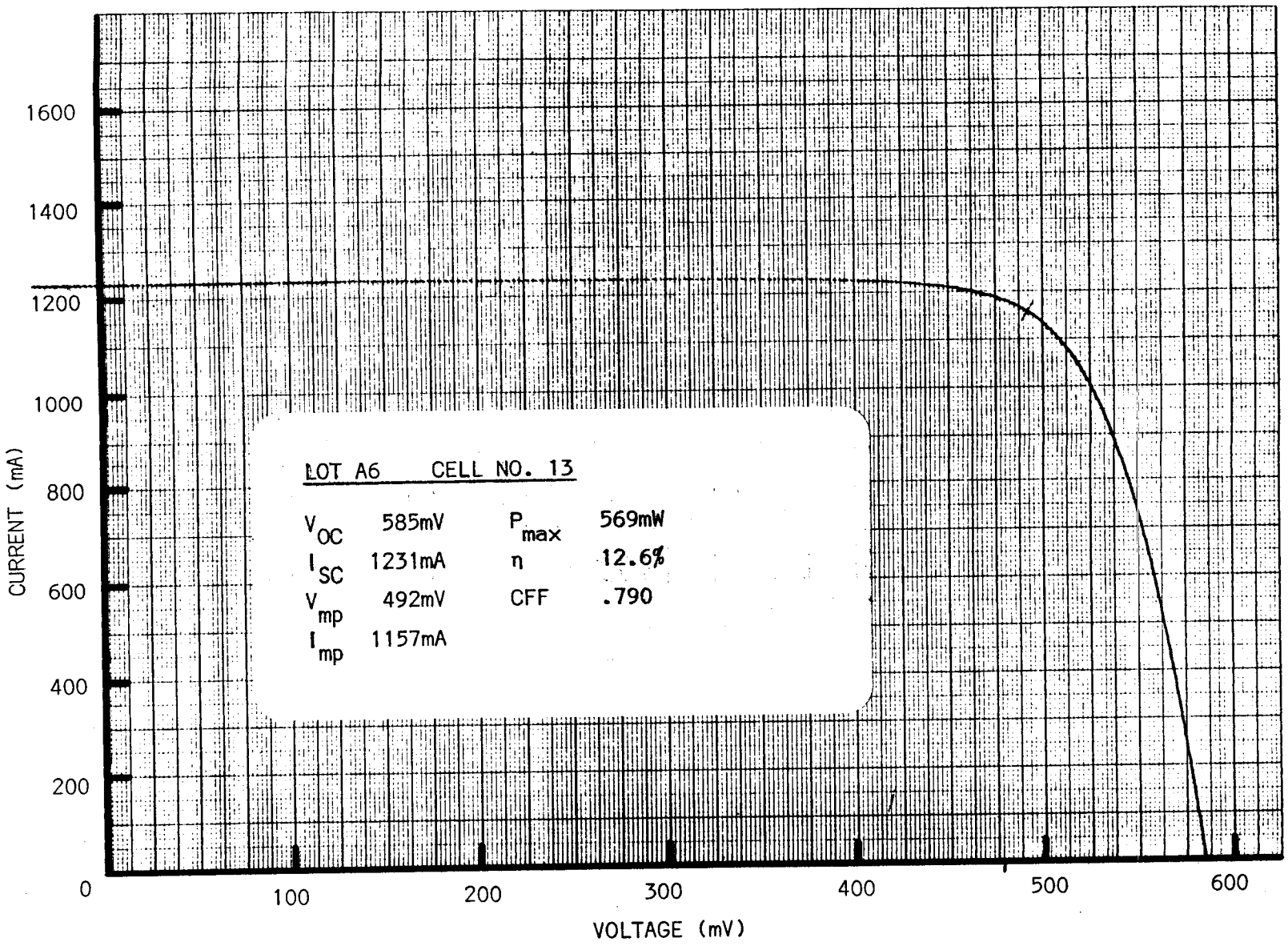

FIGURE 6: Representative AM1 current-voltage response curve for test lot no. A6.

3.0 CONCLUSIONS AND RECOMMENDATIONS

A general summary of the data presented in this report might be that the test lots behaved exactly as expected and created a firm baseline from which processing variations and device structure changes can be implemented and evaluated. The cell performance as a function of thickness as given in Table 2 is in excellent agreement with previously published theoretical (1) and empirical (2) work. Thus a good foundation has been established which can lead to processing and performance improvements.

A number of specific conclusions can be drawn. As exhibited in Table 2, power output falls off directly in relation to cell thinness for the simple n-on-p baseline structure. Differences in power output data for each test lot must be tempered slightly by the effect of differences in the resistivity of the cell substrates. For example, a change from 1.0 Ω-cm to 1.5 Ω-cm will result in a decrease in open circuit voltage of about 9 mV. This is especially important in comparing lot A1 (2.34 Ω-cm) with respect to the other lots.

Processing yield, at least for this first trial, also falls off with wafer thinness. However, this conclusion is not irrevocable. Additional processing experience and changes in handling techniques may minimize the difference between thin and thick substrates. The fact that material characteristics and handling are both very important to yield can be proven by considering the 14 mil thick wafers of lot A1. This lot was completed with a lower yield than that of three other lots of 7 and 8 mil thick wafers.

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(1) H. J. Hovel, Semiconductors and Semimetals, Volume 11, Solar Cells, Academic Press, New York, 1975, Chap. 5.

(2) C.F. Gay, "Thin Silicon Solar Cell Performance Characteristics," Proceedings of the Thirteenth IEEE Photovoltaic Specialists Conference, 1978, p. 444.

The baseline diffusion process which was used for lots A1 through A6 resulted in very uniform short circuit current and open circuit voltage values for cells within a lot. Among these six lots, the worst standard deviation for current was 1% and the worst for voltage was 0.7%. Actually, much of this small deviation can be shown to be due to variations in substrate resistivity within a lot.

4.0 PLANS

For the coming quarter the program plan is expected to proceed on schedule. Further studies will be initiated to compared advanced cell structures utilizing various combinations of surface preparations, back surface fields, back surface optical reflecitons, and ion-implanted impurity layers. Samples will be prepared for determining the optimum thickness of saw damage removal from as-cut, wire-sawed wafers. An initial analysis of wafering and processing yields will be formulated and related to cell performance and cost.

5.0 NEW TECHNOLOGY

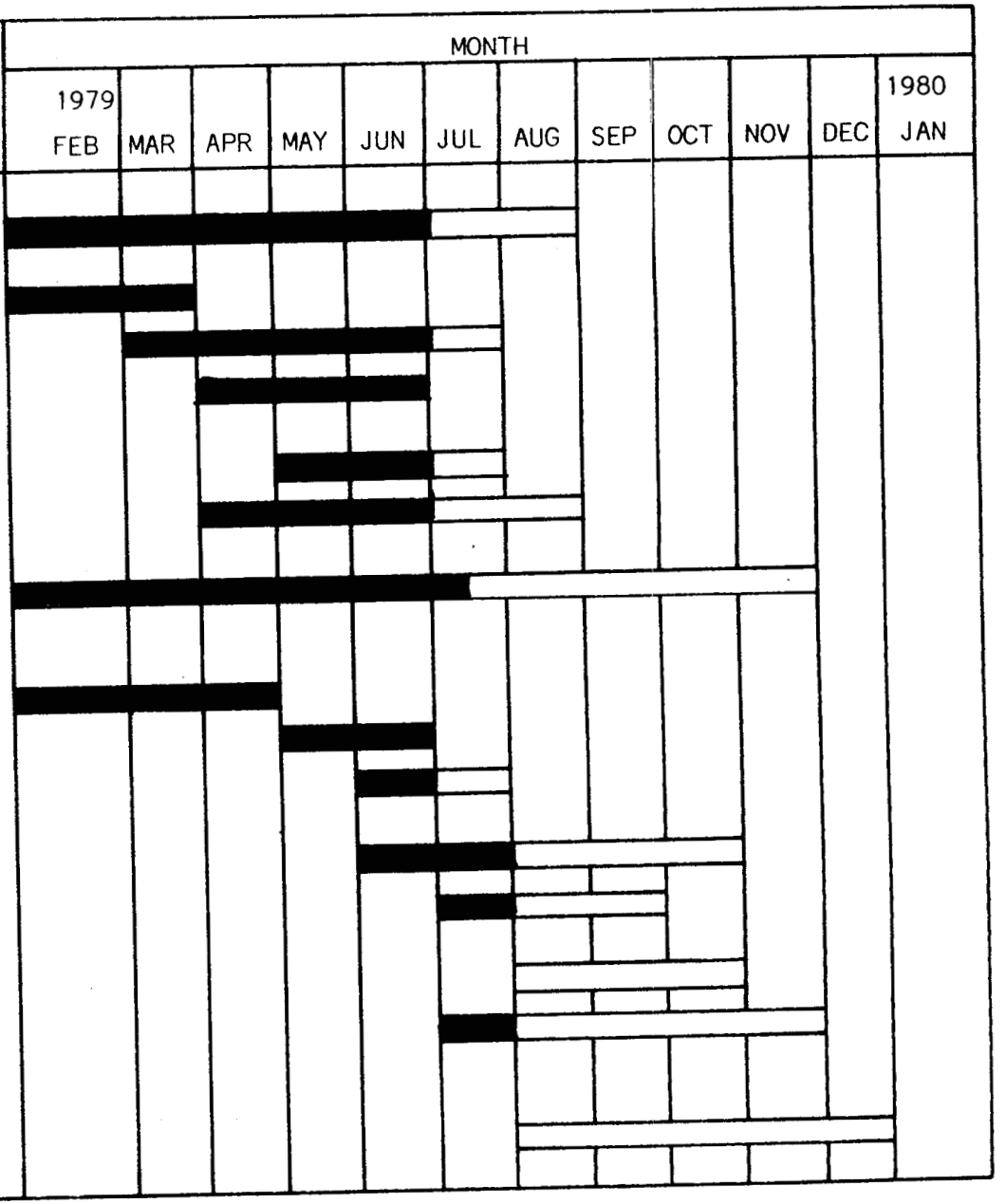
No reportable items of new technology have been identified, as yet.

6.0 PROGRAM AND DOCUMENTATION MILESTONES

Activities associated with the total program are shown in the Program and Documentation Milestone Charts, Figures 1 and 2 contained in Appendix 1.

APPENDIX I

Program Milestone Chart



Task 1: Fabrication and evaluation of solar cells on 7 mil thick wafers

- 1a. Obtain wafers
- 1b. Fabricate cells
- 1c. Characterize processing difficulties
- 1d. Modify processing
- 1e. Analyze cell characteristics

Task 2: Obtain and process wafers sawed to 5 mils thickness and etched to 4 mils

- 2a. Obtain wire-saw guides
- 2b. Obtain wafers
- 2c. Yield analysis of wafer preparation
- 2d. Fabricate cells
- 2e. Characterize processing difficulties
- 2f. Modify processing
- 2g. Analyze cell characteristics

Task 3: Evaluate the possibility of thinner cells

Figure 1

Program Milestone Chart (Continued)

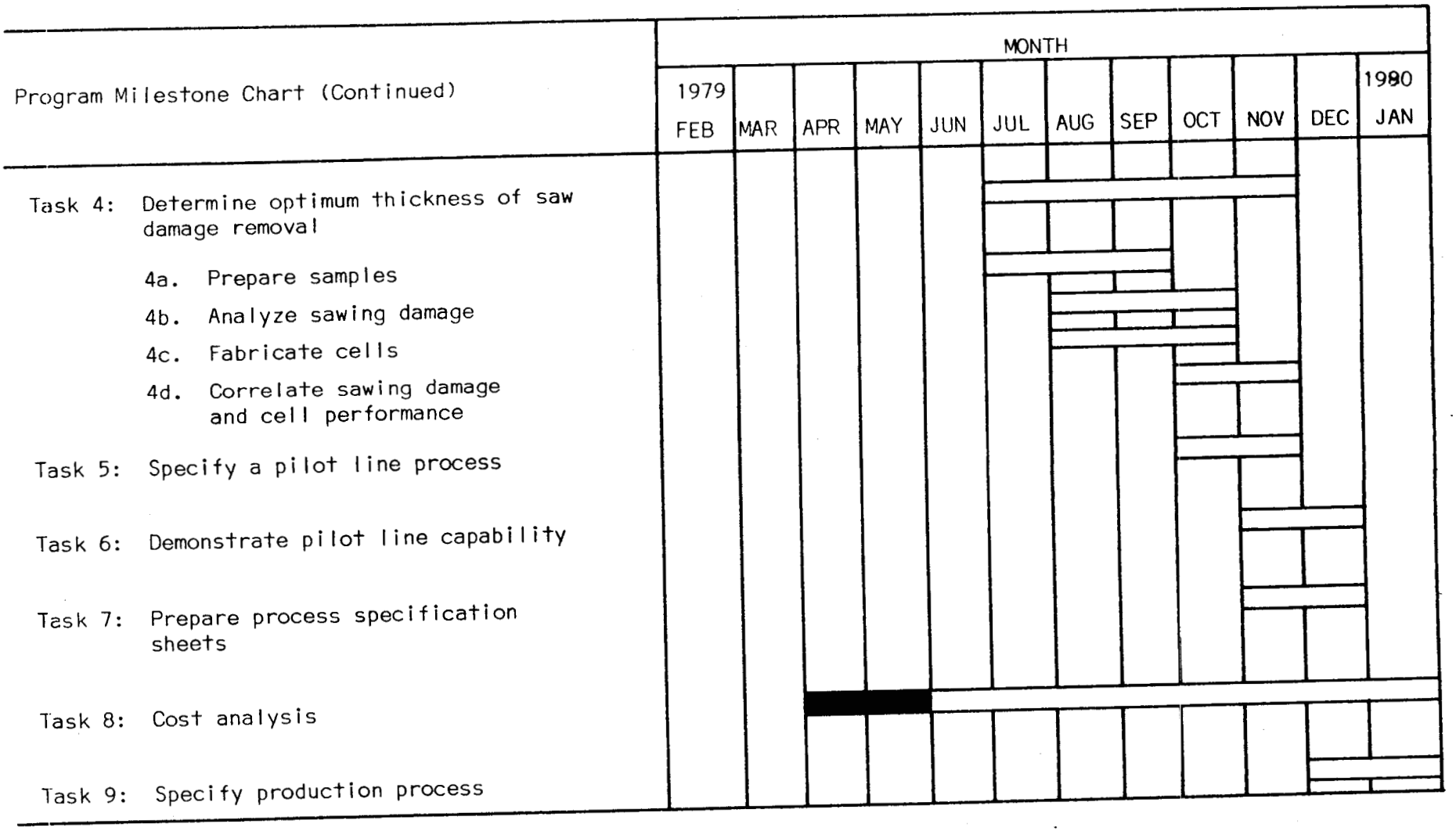


Figure 1 (Continued)

Documentation Milestone Chart

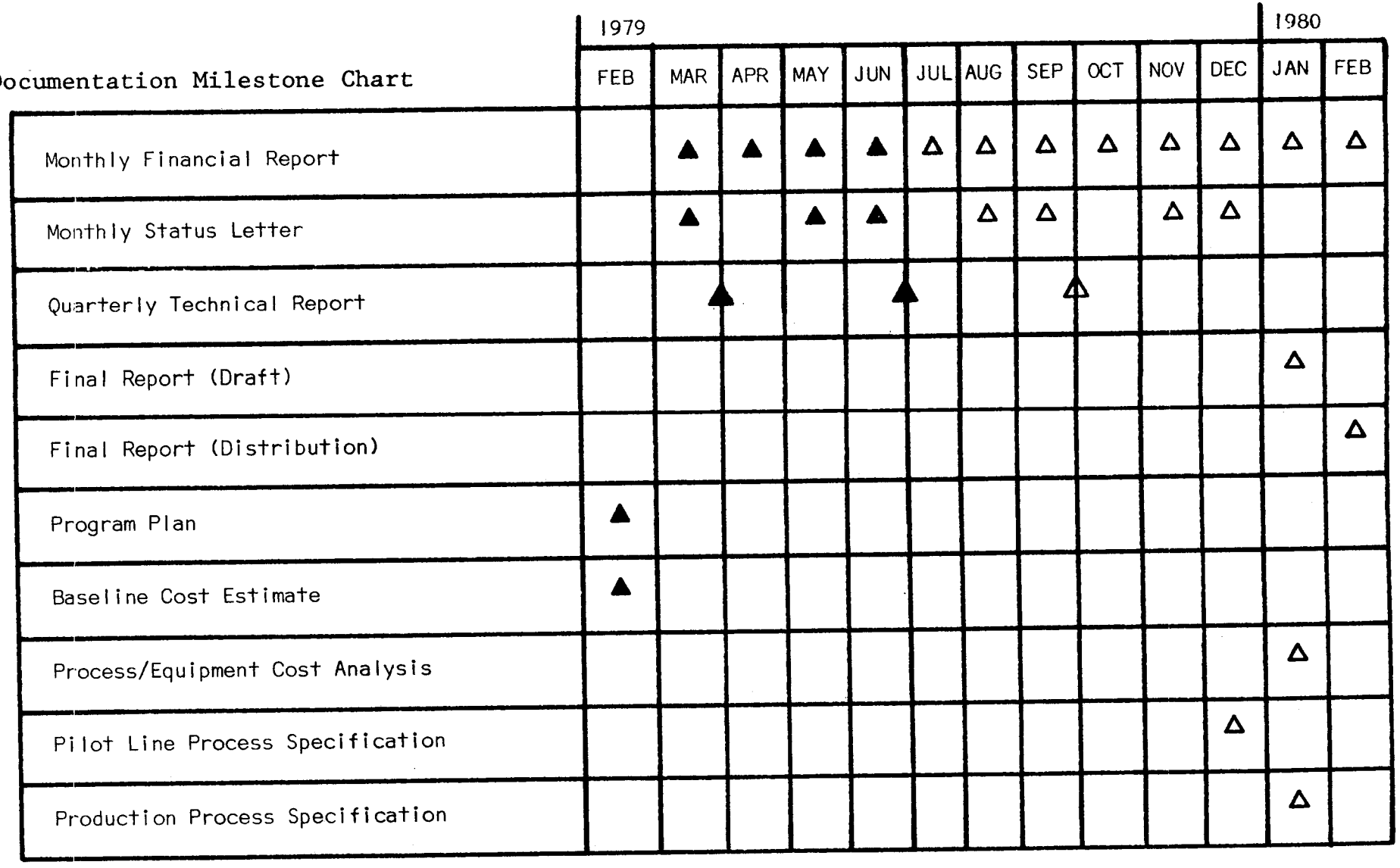


Figure 2